

Notice of References Cited

Application/Control No.

10/084,383

Applicant(s)/Patent Under

Reexamination

SNIDER, GREGORY STUART

Examiner

Phallaka Kik

Art Unit

2825

Page 1 of 3

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,360,191	03-2002	Koza et al.	703/6
	B	US-6,128,770	10-2000	Agrawal et al.	716/17
	C	US-6,099,583	08-2000	Nag, Sudip K.	716/16
	D	US-6,086,631	07-2000	Chaudhary et al.	716/16
	E	US-5,959,871	09-1999	Pierzchala et al.	703/4
	F	US-5,850,537	12-1998	Selvidge et al.	716/12
	G	US-5,835,751	11-1998	Chen et al.	716/16
	H	US-5,740,069	04-1998	Agrawal et al.	716/16
	I	US-5,640,327	06-1997	Ting, Benjamin S.	716/7
	J	US-5,598,346	01-1997	Agrawal et al.	716/16
	K	US-2003/0028852	02-2003	Thurman et al.	716/12
	L	US-2002/0157066	10-2002	Marshall et al.	716/1
	M	US-6,584,601	06-2003	Kodosky et al.	716/4

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	WO 9833182 A1	07-1998	World Intellect	MARSHALL et al.	G11C 08/00
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Brown et al., "A Detailed Router for Field-Programmable Gate Arrays", 1990 IEEE International Conference on Computer-Aid Design, 11 November 1990, pp. 382-385.
	V	Wu et al., "Graph Based Analysis of FPGA Routing", Proceedings of European Design Automation Conference, 1993, with EURO-VHDL, 20 September 1993, pp. 104-109.
	W	Chang et al., "FPGA Global Routing Based on a New Congestion Metric", Proceedings of 1995 IEEE International Conference on Computer Design: VLSI in Computers and Process, 2 October 1995, pp. 372-378.
	X	Chrzanowska-Jeske et al., "Partitioning Approach to Find an Exact Solution to Fitting Problem in an Application-Specific EPLD Device", Proceedings of Design Automation Conference, 1993, with Euro-VHDL '93, 20 September 1993, pp. 39-44.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited

Application/Control No.

10/084,383

Applicant(s)/Patent Under

Reexamination

SNIDER, GREGORY STUART

Examiner

Phallaka Kik

Art Unit

2825

Page 2 of 3

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,536,018	03-2003	Chisholm et al.	716/4
	B	US-6,317,804	11-2001	Levy et al.	710/305
	C	US-5,659,484	08-1997	Bennett et al.	716/16
	D	US-5,519,629	05-1996	Snider, Gregory S.	716/17
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Ejnioui et al., "Routing on Switch Matric Multi-FPGA Systems", Thirteen International Conference on VLSI Design, 03 January 2000, pp. 248-253.
	V	Sun et al., "Routing for Symmetric FPGAs and FPICs", 1993 IEEE/ACM International Conference on Computer-Aided Design, November 1993, pp. 486-490.
	W	Hauck et al., "Mesh Routing Topologies for Multi-FPGA Systems", Proceedings of IEEE International Conference on Computer Design: VLSI in Computers and Process, 10 October 1994, pp. 170-177.
	X	Wu et al., "Not Necessarily More Switches Mor Routability", Proceedings of the ASP-DAC '97 Asia and South Pacific Design Automation Conferenc , 28 January 1997, pp. 579-584.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 10/084,383	Applicant(s)/Patent Under Reexamination SNIDER, GREGORY STUART	
	Examiner Phallaka Kik	Art Unit 2825	Page 3 of 3

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chang et al., "A Graph-Theoretic Sufficient Condition for FPGA/FPIC Switch-Module Routability", Proceedings of 1997 IEEE International Symposium on Circuits and Systems, 9 June 1997, Vol. 3, pp. 1572-1575.
	V	Wang et al., "Graph-Based Detailed Router for Hierarchical Field-Programmable Gate Arrays", IEE Proceedings of Computers and Digital Techniques, Vol. 146, No. 1, January 1999, pp. 57-67.
	W	Alexander et al., "High-Performance Routing for Field-Programmable Gate Arrays", Proceedings of Seventh Annual IEEE International ASIC Conference and Exhibit, 19 September 1994, pp. 138-141.
	X	Wu et al., "Graph Bas d Analysis of 2-D FPGA Routing", IEEE Transactions on Computer-Aided Design of Int grated Circuits and Systems, Vol. 15, No. 1, January 1996, pp. 33-44.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.